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APPL NO.	FILING OR 371 (c) DATE	ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	DRAWINGS	TOT CLMS	IND CLMS
10/634,636	08/04/2003	2818	774	UNTP020	10	56	2

CONFIRMATION NO. 7199

22434  
 BEYER WEAVER & THOMAS LLP  
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CORRECTED FILING RECEIPT



\*OC000000012301867\*

Date Mailed: 04/07/2004

Receipt is acknowledged of this regular Patent Application. It will be considered in its order and you will be notified as to the results of the examination. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections, facsimile number 703-746-9195. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

**Applicant(s)**

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**Assignment For Published Patent Application**

Unity Semiconductor Corporation, Sunnyvale, CA;

**Domestic Priority data as claimed by applicant**

This application is a CIP of 10/249,846 05/12/2003  
 which claims benefit of 60/400,849 08/02/2002  
 and claims benefit of 60/422,922 10/31/2002

**Foreign Applications**

If Required, Foreign Filing License Granted: 11/03/2003

Projected Publication Date: Request for Non-Publication Acknowledged

Non-Publication Request: Yes

Early Publication Request: No

**\*\* SMALL ENTITY \*\***

**Title**

2-Terminal trapped charge memory device with voltage switchable multi-level resistance

**Preliminary Class**

365

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Title 35, United States Code, Section 184  
Title 37, Code of Federal Regulations, 5.11 & 5.15**

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